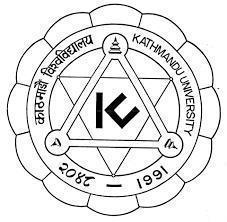
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**A Mini Project Report**

**on**

**“SPAN COMPUTER DESIGN”**

**[Code No: COMP 315 ]**

**(For partial fulfillment of 3rd Year/1st Semester in Computer Engineering)**

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**Submission Date:2024/06/8**

# **ACKNOWLEDGEMENT**

We are grateful for the opportunity to participate in this project. We would like to express our sincere gratitude to our esteemed teacher, Mr. Pankaj Dawadi, for incorporating this mini-project into our COMP 315 syllabus. We appreciate the chance to explore and enhance our skills and knowledge in computing. We have tried to deliver our best in this project.

Sincerely,

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**Chapter 2: Design Considerations**

As we know, the computer understands as well as executes the operation in binary

code. This binary code is called the instruction. A computer can understand and

execute a few numbers of instructions that are hardwired in its design, these

instructions form the instruction set of the computer. The selection of binary code for

the instruction and the instruction itself is the main task of the computer designer.

Designing an 22 bit CPU is a complex and yet essential process needed to

implement all the ideas of Computer System Architecture together. A thorough

understanding of computer organization and architecture is necessary to complete

this task.

On our computer, we have implemented different instructions based on the

suitability of our project. Our computer has a 4-bit opcode, 16-bit address length and

2-bit addressing mode.

Our computer consists of the following hardware components:

1. A memory of 65536 x 22.

2. Nine registers: AR(16), PC(16), DR(22), AC(22), IR(22), TR(22), OUTR, INPR and SC.

3. Six flip-flops: R, S, E, IEN, FGI and FGO.

4.Three decoders: a 4x16 opcode decoder, a 4x16 timing decoder and a 2x4

addressing mode decoder.

5. A 22-bit common bus.

6. Control logic gates.

7. Adder and logic circuit connected to the input of AC.

This section outlines the design process, internal architecture, and instruction set of our computer.

2.1. Instruction Format

An instruction is divided into three parts:

Operation Code (Opcode): It specifies the operation for an instruction.

Address: It specifies the registers and/or memory locations used in an operation.

In the SPAN computer, memory contains 65536(2^16) words, requiring 16 bits to specify an address. Each word is 22 bits, with 16 least significant bits (LSBs) reserved for the address, the 2 most significant bits (MSBs) for addressing modes, and the remaining 4 bits for opcodes.

2.2. Addressing Modes

The SPAN computer uses two addressing modes:

|  | Addressing Mode Field | Addressing Mode |
| --- | --- | --- |
| I0 | 00 | Direct Addressing Mode |
| I1 | 01 | Indirect Addressing Mode |
| I2 | 10 | Register Reference Instruction Mode |
| I3 | 11 | Input Output Instruction Mode |

2.2.1. Direct Addressing Mode

The address of the operand is stored in the memory location specified in the instruction in the direct addressing mode.

2.2.2. Indirect Addressing Mode

The address of the operand is stored within the instruction itself in the indirect addressing mode.

2.3. Components

**2.3.1. Registers**

The SPAN Computer has nine registers:

Instruction Register (IR)

*Size: 18 bits*

IR holds 22 bits of instruction read from memory. The address in the PC is transferred to the Address Register (AR), and the content of the memory location pointed to by the AR is then transferred to the IR via the common bus system (CBS). The instruction is decoded to provide the necessary control signals for execution.

Program Counter (PC)

Size: 16 bits

It contains the address of the next instruction to be executed. When a byte (machine code) is fetched, the PC is incremented by one. So that it can fetch the next instruction. If the computer is reset or restarted, the program counter returns to zero value. For subroutines, the PC is saved and loaded with the subroutine's address, resuming with the saved address after the subroutine call.

Data Register (DR)

Size: 22 bits

It stores the operand read from memory to be processed. The output of the DR is an input to the Arithmetic and Logic Unit (ALU).

Accumulator (AC)

Size: 22 bits

It stores the result of operations. The input comes from the ALU's output and the out of the operation gets stored in the accumulator.

Input Register (INPR)

The Input Registers (INPR) holds the input characters given by the user.

Output Register (OUTR)

The Output Registers (OUTR) holds the output after processing the input data.. The output can be connected to an external display.

Temporary Register (TR)

Size: 22 bits

It holds data during arithmetic and logic operations. It is non-programmable and used for intermediate results.

Sequence Counter (SC)

Size: 4 bits

It is used to generate different Timing Signals. It is connected to a 4x16-bit decoder.

Address Register (AR)

Size: 22 bits

It is needed by processor to keep track of which locations in memory it is pointing. Denoted by

AR.

**2.3.2. Arithmetic and Logic Unit (ALU)**

The ALU performs arithmetic and logical operations. It has the ability to perform all processes related to arithmetic and logic operations such as addition, subtraction, and shifting operations, including Boolean comparisons.

**2.3.3. Memory Unit**

*Size: 65536 x 22*

SPAN Computer has 65536 slots where 22 bit of instructions can be stored and executed in each slots. The memory receives its address from the AR and data from the Control Bus System, with read/write operations determined by control signals.

**2.3.4. Common Bus System**

The SPAN computer has nine registers ,a memory unit, and a control unit. The bus has a memory unit with 65536 slots each of 22 bits , Accumulator of 22 bits, Address Register of 16 bits, Program Counter of 16 bits , Instruction Register of 22 bits, Data Register of 22 bits and Temporary Register of 22 bits. Status Signals are used to choose particular registers or memory location for the Common bus system.Initially Address for the instruction to be executed is extracted from the Program Counter and then passed to Address Register through bus and then the data is fetched from memory and passed that data to the data register and though ALU specific operation is performed.

Path to transfer information from one register to another and between memory and register is shown in the figure below.

**2.3.5. Flip Flops/Flags**

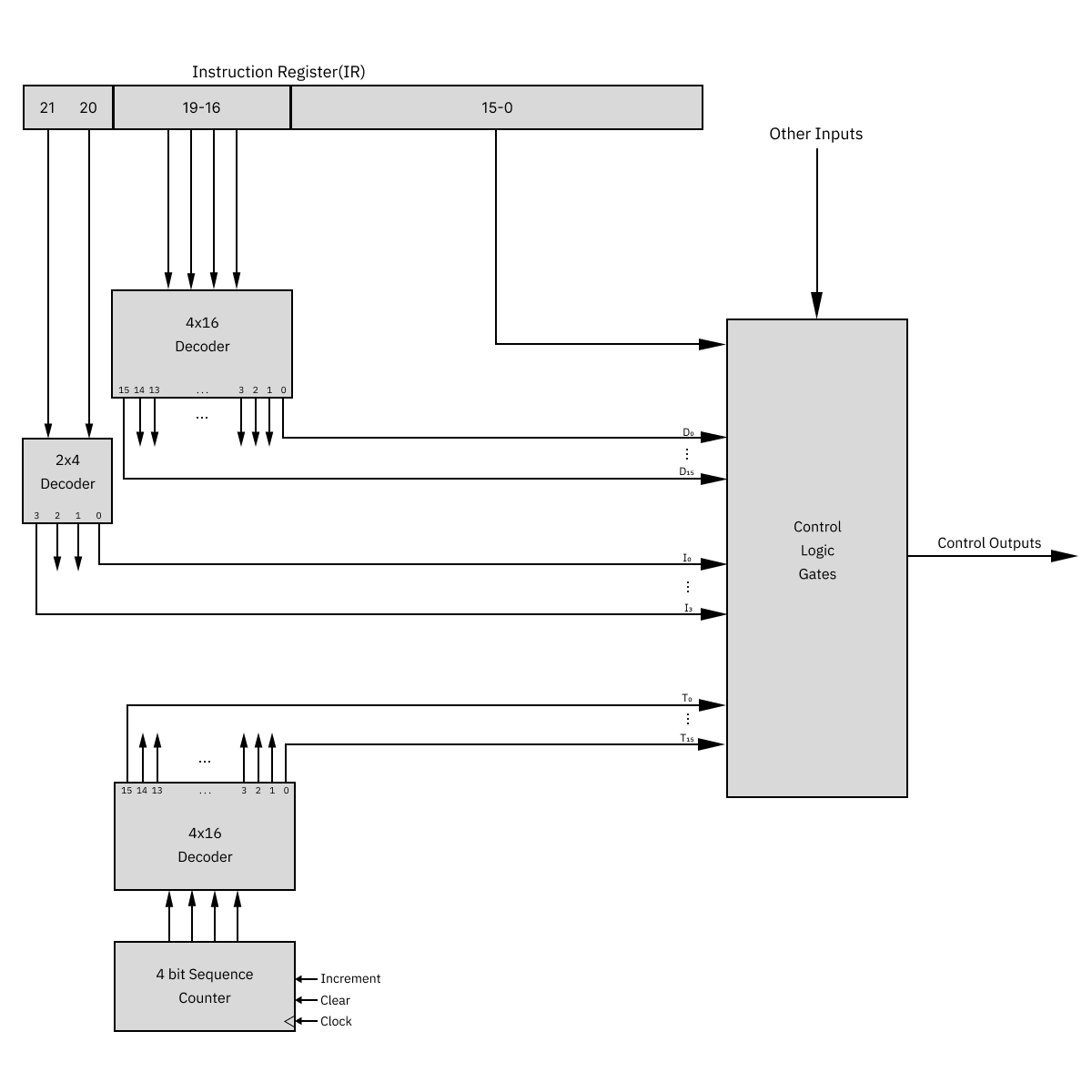
There are 6 flip flops used in SKIP Computer which are listed below.

| Flipflop | Description |
| --- | --- |
| S | Start Stop Flip Flop |
| R | Interrupt Flipflop |
| E | End Around Carry |
| FGI | Input Flag |
| FGO | Output Flag |
| IEN | Interrupt Enable |

**2.3.6. Control Unit**

The Control Unit (CU) generates the necessary control and timing signals to carry

out the sequences of micro-operations to execute the given instruction



**2.4. SPAN Instructions**

Different Types of Instructions in SPAN computer are:

* Memory Reference Instruction (MRI)

These instructions refer to the memory address as an operand. The other operand is always accumulator. 00 and 01 in Addressing modes Specifies the Memory Reference Instruction in SPAN computer.

| I | OPCODE | MEMORY ADDRESS |
| --- | --- | --- |

*Figure 7: MRI Instruction*

For Direct Addressing,

| 00 | OPCODE | MEMORY ADDRESS |
| --- | --- | --- |

*Figure 7: MRI Instruction for Direct Addressing*

For Indirect Addressing,

| 01 | OPCODE | MEMORY ADDRESS |
| --- | --- | --- |

*Figure 7: MRI Instruction for Indirect Addressing*

* Register Reference Instruction (RRI)

These instructions perform operations on registers rather than memory addresses. 10 bits in Addressing mode specifies Register Reference Instruction.

| 10 | OPCODE | MEMORY ADDRESS |
| --- | --- | --- |

*Figure 7:*  *Register Reference Instruction*

* Input-Output Instruction (IOI)

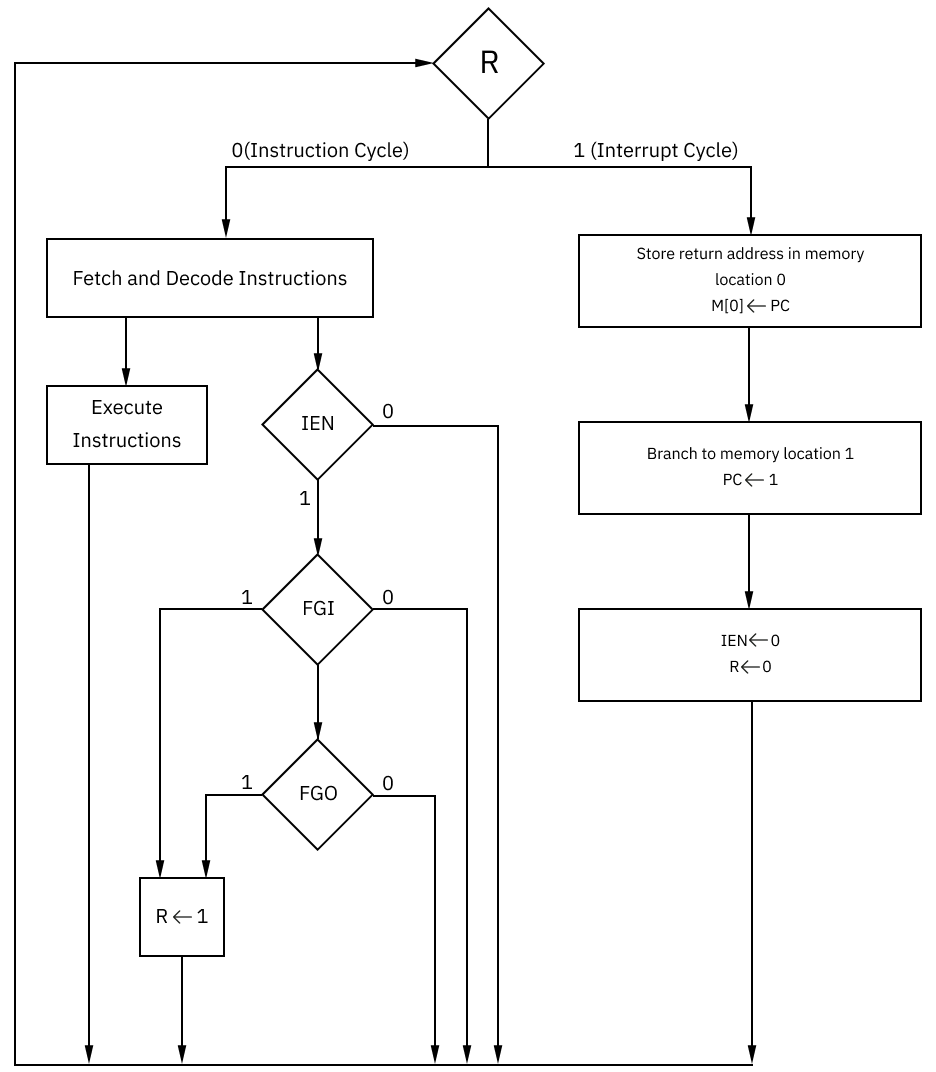
These instructions are for communication between computer and outside environment.

11 in Addressing Modes specifies Input-Output Instruction

| 11 | OPCODE | MEMORY ADDRESS |
| --- | --- | --- |

*Figure 7:*  *Input-Output Instruction*

**2.4.1 SPAN Computer Instructions**

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